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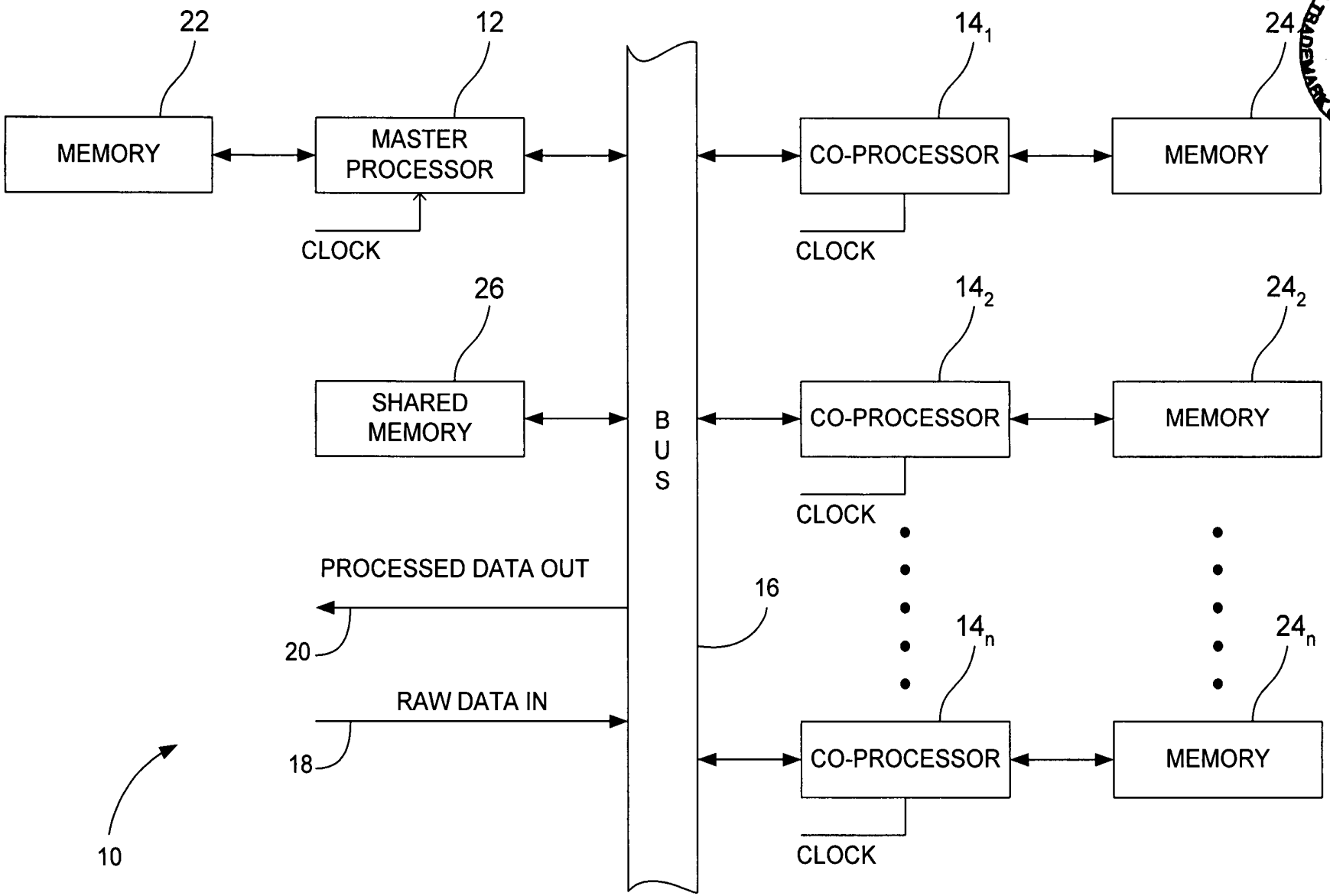

FIG. 1 (PRIOR ART)

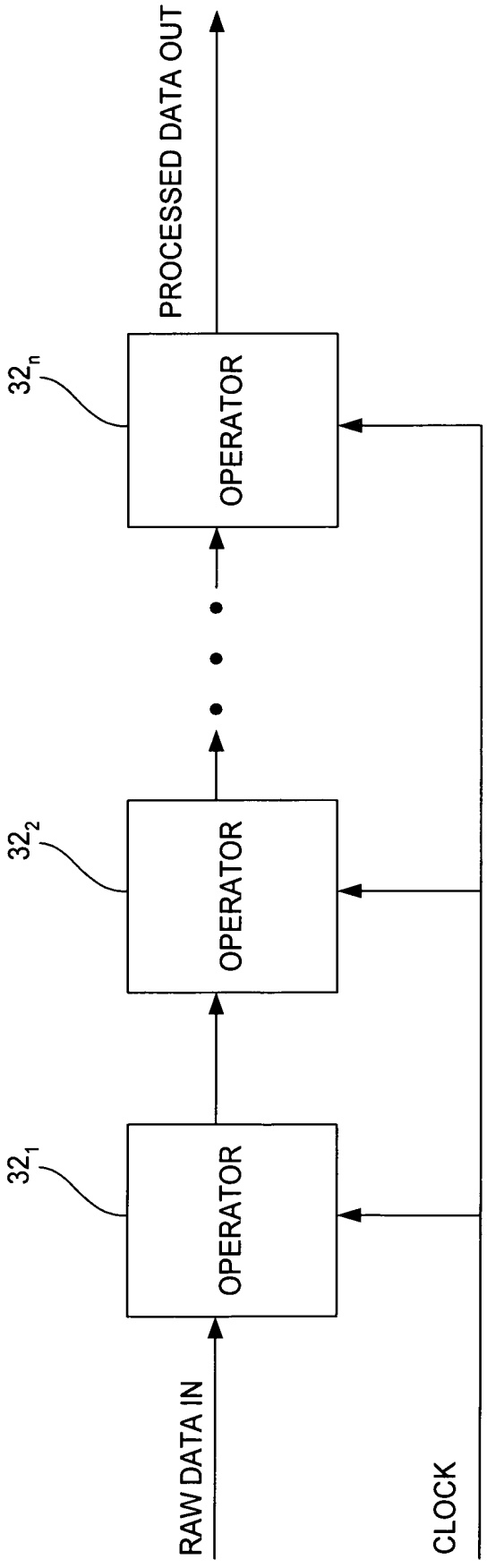
PROCESSED DATA OUT
32_n
OPERATOR
32_2
OPERATOR
32_1
OPERATOR
RAW DATA IN
CLOCK
30

FIG. 2

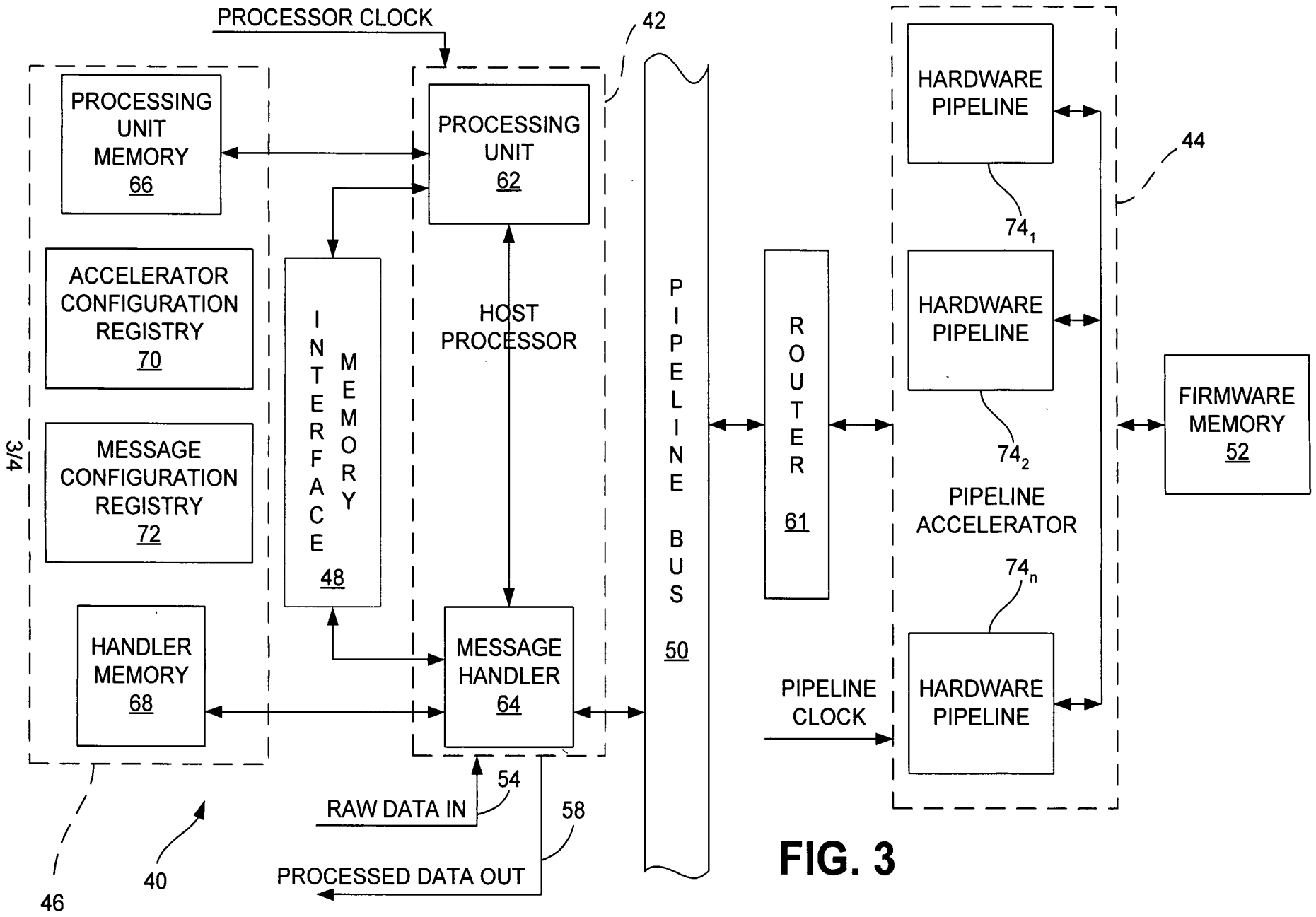
PROCESSOR CLOCK
42
PROCESSING UNIT MEMORY 66
PROCESSING UNIT 62
ACCELERATOR CONFIGURATION REGISTRY 70
INTERFACE MEMORY 48
HOST PROCESSOR
MESSAGE CONFIGURATION REGISTRY 72
HANDLER MEMORY 68
MESSAGE HANDLER 64
PIPELINE BUS 50
ROUTER 61
HARDWARE PIPELINE
HARDWARE PIPELINE
HARDWARE PIPELINE
44
74 1
74 2
74 n
PIPELINE ACCELERATOR
FIRMWARE MEMORY 52
PIPELINE CLOCK
RAW DATA IN
54
58
PROCESSED DATA OUT
46
40
3/4

FIG. 3

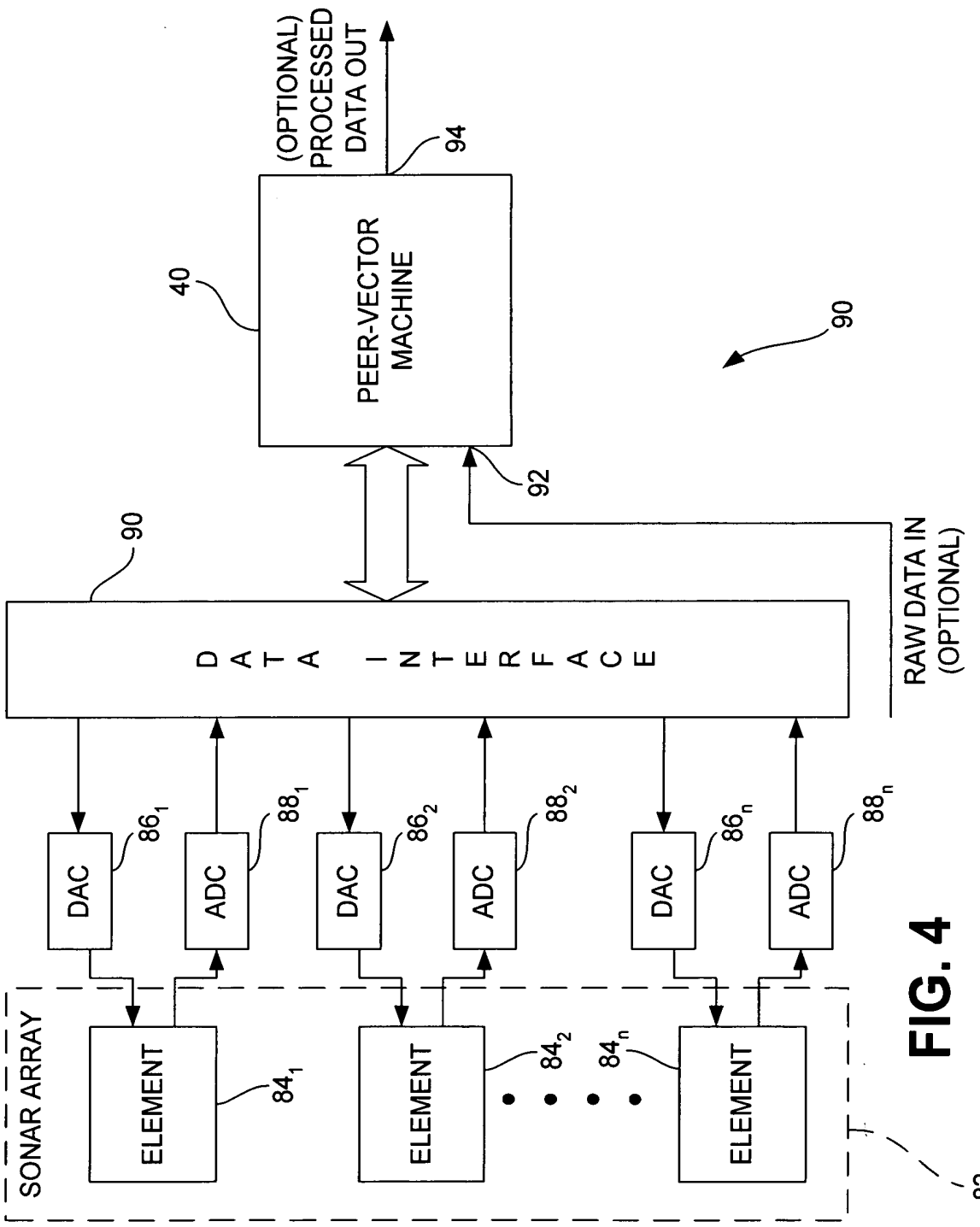
(OPTIONAL)
PROCESSED
DATA OUT
94
40
PEER-VECTOR
MACHINE
90
92
90
DATA INTERFACE
RAW DATA IN
(OPTIONAL)
DAC
86_1
ADC
88_1
DAC
86_2
ADC
88_2
DAC
86_n
ADC
88_n
SONAR ARRAY
ELEMENT
84_1
ELEMENT
84_2
84_n
ELEMENT
82

FIG. 4